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INFORMATION
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ENGINEERING PRODUCT SPECIFICATION, PART 1
PERIPHERAL SUBSYSTEM INTERFACE (PSI)

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1.0 OVERVIEW

1.1 Functionality

The Peripheral Subsystem Interface (PSI) is a transfer and control link for exchanging information between freestanding peripheral control units (PCU's) and Input/Output controllers (IOC's). Information is exchanged by controlling the logical states of various interface signal wires according to the detailed functional rules specified in this document. The PSI exists between an IOC, which accesses main storage, interprets I/O instructions and performs I/O interruptions, and a PCU which controls and operates the I/O device (see Figure 1.1).

This document is extracted from the NPL document referenced below. This interface shall be used to provide a link to the 6000 System. The interface described herein is the same as the NPL interface, but where the NPL document is oriented toward an application with NPL IOC's and processors, this document is oriented toward the 6000 processors, and IOC's (IOM, 355, etc.).

There are functional capabilities outlined in this document which may not be implemented by all users. Just because two pieces of 6000 line equipment are connected through a PSI interface per this document, does not imply complete implementation of this specification; it may be a subset. The functional capabilities utilized will be outlined in the particular subsystem documents. For example, the implementation of the PSIA for the IOM does not provide capability to suspend data dialogs, nor does it provide for putting data into memory in reverse order. So far, none of the applications on the 6000 line intend to make use of the Metering lines, MTO, or the Reserve In Line, REI, although the capability is there for future users.

1.2 Definition of Terms

Table 1.2 lists and defines terms used in this document which may require clarification.

1.3 References

NPL Product Line Plan
NPL System Objectives
NPL Peripheral Subsystem Interface, Area Objectives, NPL-AOB-IF-100
NPL Peripheral Subsystem Interface, Performance Specification,
NPL-PFS-IF-100
NPL Central Processor Functional Specification (Level 2), Sections
21-25.

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NPL Functional Specification for NPL Peripheral Subsystem Interface,
NPL-FSP-IF-100, BL 0000.
655 IOM Peripheral Subsystem Interface Adapter, EPS-1, #43A177880.

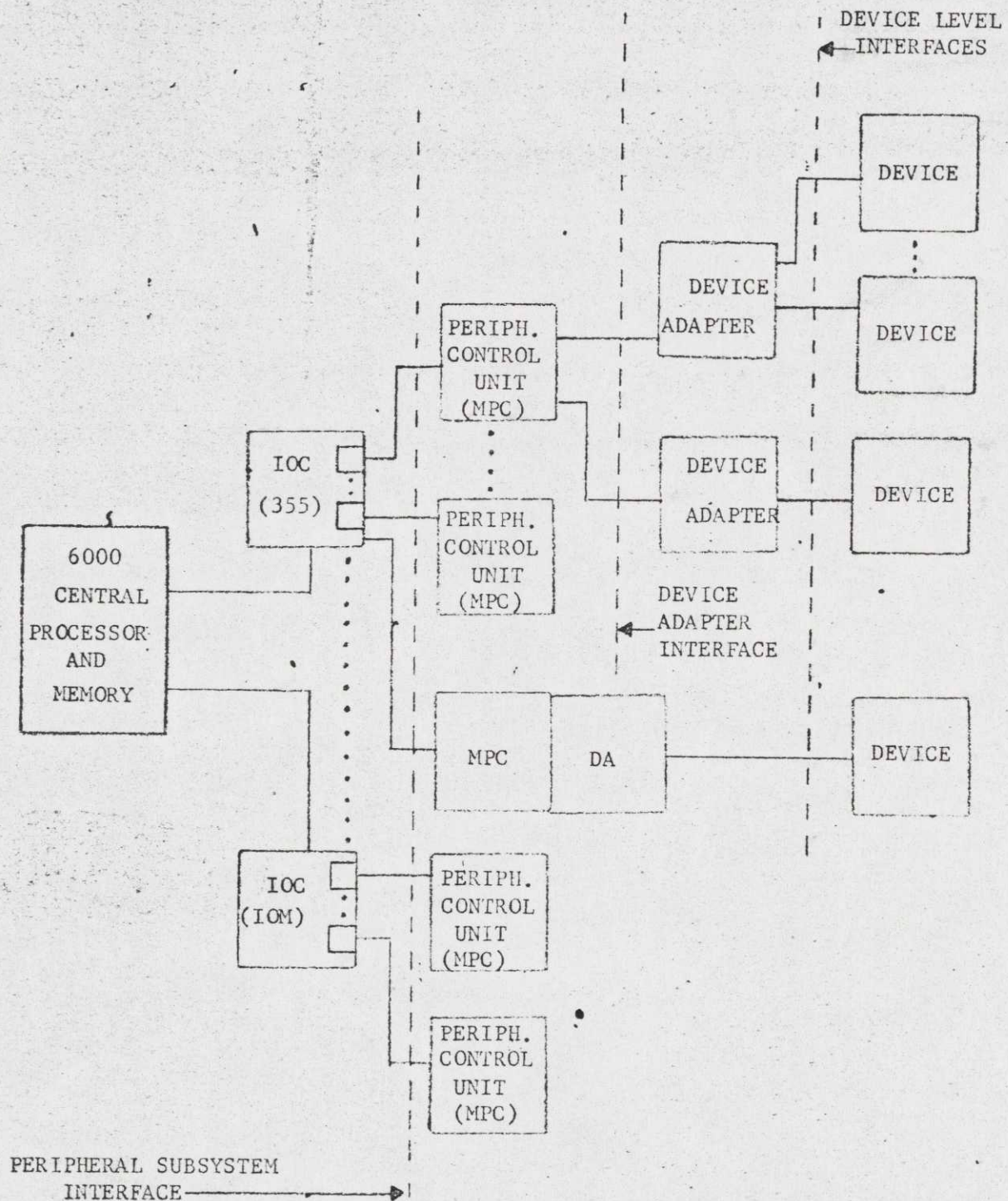


FIGURE 1.1. INTERFACE LOCATION ON 6000 SYSTEMS

TABLE 1.2 GLOSSARY OF TERMS

<u>TERMS</u>	<u>DEFINITIONS</u>
Bootload	The process which loads from a peripheral device into main memory the information necessary for normal execution of programs, after the system has been initialized (bootload in). Other terms with similar meanings are Bootstrap, Initial Memory Load (IML), Initial Memory Transfer, and Initial Program Load (IPL).
Burst Mode	The normal mode of information transfer operations over the PSI for high speed peripheral devices. In this mode of information transfer, all the bytes being transferred are associated with the same logical channel and are not interrupted by control information transfer sequences or data transfer sequences for other logical channels.
Byte Wide Path	Bytes of information transferred across the interface consist of eight information bits plus one odd parity bit (see Figure 1.2.1). The information is arranged so that bit 7 is always the least significant bit. The parity bit is ONE if the number of ONE bits in the corresponding eight information bits is even, ZERO if the number of ONE bits is odd, i.e., odd parity is generated on the eight information bits.

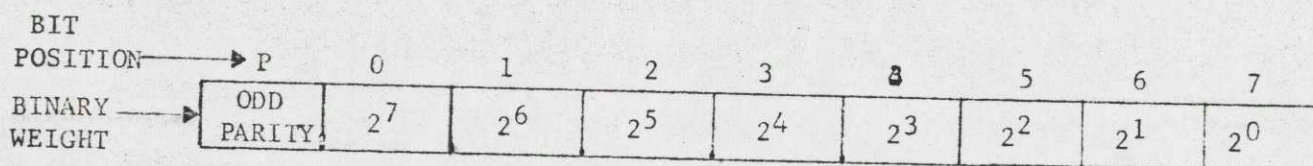


FIGURE 1.2.1 EIGHT BIT BYTE

(Reference definition of "Byte Wide Path" in Table 1.2).

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TABLE 1.2 (Continued)

<u>TERMS</u>	<u>DEFINITIONS</u>
Central Processor Complex (CPC)	The Central Processor Complex consists of those units used for addressing main storage, for retrieving or storing information, for arithmetic and logic processing of data, for sequencing instructions in the desired order, and for initiating the communication between storage and external devices. The main units of the CPC are the Central Processor Unit (CPU), the main memory and the Input/Output Controller (IOC, IOM, etc).
Channel Program (CP)	A complete set of instructions and addressing information to carry out an I/O operation. It is composed of a DCW list.
Input/Output Controller (IOC)	The mainframe hardware/firmware involved during the execution of a channel program. It may control several physical channels. In this document, the unit which connects to the mainframe side of the PSI is referred to as the IOC. Other terms that have been used with the same meaning in this context are Central Processor Unit, Channel Control Unit, Channel, I/O Processor, IOM, 355, etc.
IOC Instruction	An instruction sent from the IOC to the PCU. This instruction is not part of the channel program, but may be related to channel program activity (e.g., abort, disconnect).
Line States	An interface signal line in the ONE state, or high, is understood to be in the logical TRUE state; a line in the ZERO state, or low, is understood to be in the logical FALSE state. The rise of a line will imply a transition from the FALSE to the TRUE state, while the fall of a line will imply the transition from the TRUE to the FALSE state.
Logical Channel (LC)	The PSI is based on the concept of logical channels. The access path from the CPU to the device for the purpose of executing an I/O operation is termed a channel. The channel consists of IOC facilities, a hardware link between the IOC and PCU identified as the physical channel, and a logical channel. The logical channel in its most elementary form is the

TABLE 1.2 (Continued)

<u>TERMS</u>	<u>DEFINITIONS</u>
Logical Channel (continued)	collection of facilities in a peripheral control unit subsystem required to execute an I/O operation such as a read, write, etc. An I/O operation is defined by a channel program. A logical channel can only have one channel program active on it at one time. Logical channel numbers are used by the channel for ordering the storage of parameters required to maintain a number of channel programs operating simultaneously. As such, software visibility of an I/O operation is through a logical channel. (From a software point-of-view, devices are allocated an IOC number, a physical channel number and a logical channel number for selection purposes.) A logical channel number explicitly identifies a device. A channel program is restricted to one device. Devices are assigned logical channel numbers at system configuration time or when the device is added to the system. There may be more than one logical channel per device.
Multiplex Mode	The normal mode of information transfer over the PSI where several low speed devices are attached to a single PCU. Information being transferred in this mode is associated with two or more logical channels. Service code sequences are used between the transfers to identify the logical channel the transfer pertains to.
Peripheral Control Unit (PCU)	The unit which is connected on the peripheral side of the PSI. Other names with similar meanings are Peripheral Processor, Peripheral Controller, Microprogrammed Peripheral Controller (MPC), Multi-Line Controller (MLC), etc.
Peripheral Device	A single addressable data source or sink. The peripheral device may be a unit controlling a physical medium (e.g., disc drive, tape drive) or an electronic medium (e.g., communications channel).
Peripheral Subsystem	Those functional units existing outside of the central processing and main memory facilities which are required to operate and control the peripheral devices in a system. A peripheral subsystem may include one or more PSI's, one or more peripheral control units, and one or more peripheral devices.

TABLE 1.2 (Continued)

<u>TERMS</u>	<u>DEFINITIONS</u>
Physical Channel	The hardware link between the IOC and the peripheral control unit. This hardware link consists of one PSI and the facilities at each end of the PSI dedicated to the PSI.
Read	Indicates the direction of dialog flow (from the PCU to the IOC), i.e., an input operation.
Service Code	An eight-bit instruction (plus parity) transferred over the PSI from the PCU to the IOC and used for defining subsequent information transfer over the interface as well as initiating activity in the IOC.
Write	Indicates the direction of dialog flow (from the IOC to the PCU), i.e., an output operation.
Data Chain Data Chaining	A sequence of IOTP or IONTP DCW's. (Scatter/Gather)
DCW	Data Control Word.
IDCW	Instruction DCW.
IOTP	DCW type: I/O transfer and proceed.
IONTP	DCW type: I/O non-transfer and proceed.

2.0 GENERAL DESCRIPTION

2.1 Basic Definition

The PSI is a set of signal conductors used to interconnect NPL IOC's and PCU's in a nonsymmetrical, star (radial) configuration. Within the PSI family of three interfaces, differences exist only in the number of byte wide paths. Control lines and dialogs (relationships of signals on the interface) are identical for all three interfaces, except where noted.

Interface dialog sequences are identified by service codes. Use of service codes minimizes the requirement for separate sequence identifier lines, and provides the flexibility to implement future I/O control sequences not yet conceived of (e.g., defining new service codes).

The PSI uses a fully interlocked dialog technique for which implementation is relatively simple. There are no signal skewing considerations for the equipment on either end of the interface.

The PSI normally multiplexes data on a burst basis. Each burst of data is variable in length and may consist of one or more messages and/or logical records from media as well as any part of a message or record. A burst of data may in fact consist of only one byte (i.e., byte multiplexing). Control sequences transferred over the interface separate the data transfer sequences and serve to identify and initiate subsequent activity in the attached control units as well as providing channel program addressing and channel program control information.

2.2 Timing Restrictions

There are no timing restrictions except for Reset Out (RSO), the only interface line implemented as a pulse. The interlocked nature of the interface dialog provides skew protection automatically (for greater than a minimum cable length) and eliminates the need for one-shot or other timing circuits.* There are no pulses to lose. The interface will run as fast as the slowest party on it, being self-adjusting for the speed of the equipment. The interface will run faster for a short cable and slower for a long cable, always self-adjusting.

*The minimum cable length is a function of skews for any given implementation of the interface.

2.3 Data Paths

The three interfaces in the PSI family differ only in the number of byte wide paths. An interface can be one, two, or four bytes wide. These data paths are bidirectional. A one byte wide interface consists of Data Path 1, a two byte wide interface of Data Paths 1 and 2, and a four byte wide interface of Data Paths 1, 2, 3 and 4. The highest order byte is designated Data Path 1.

Data Path 1 can carry service codes, data, commands, status, logical channel (LC) numbers, branch arguments (BA's), and IOC instructions. Data Path 2 can carry all of the above except service codes and branch arguments. Data Paths 3 and 4 can carry the same information as Data Path 1 except for LC numbers, service codes and IOC instructions. The syntax used depends on the width of the data paths, and is defined in Section 3, Service Codes.

There are no lines used to indicate data alignment for a two or four byte interface.

Normally, all data will be aligned left justified; but when data is put in memory in reverse order, the data shall be right justified (see Figure 2.3.1). Alignment is indicated by the IDCW.

Whenever more than one byte of information is transmitted, the bytes are not split in a field but are contiguous either left or right justified (as implied by the IDCW). Multiple-byte wide interfaces require that additional lines be defined to indicate which data paths carry information and which are not used during any single transfer dialog. These lines are the Data Width lines. On a two byte wide interface, there is one bidirectional Data Width line. On a four byte wide interface, there are two bidirectional Data Width lines and one bidirectional Data Width Parity line.

2.4 Interface Signal Lines

Figure 2.4.1 identifies the NPL PSI interface lines and their corresponding abbreviations, and Table 2.4.1 lists the number of lines for the different width interfaces.

All lines with the designation IN originate at the peripheral control unit and terminate at the IOC. All lines with the designation OUT originate at the IOC and terminate at the PCU. Dialog sequences are illustrated in Sections 3 and 4.

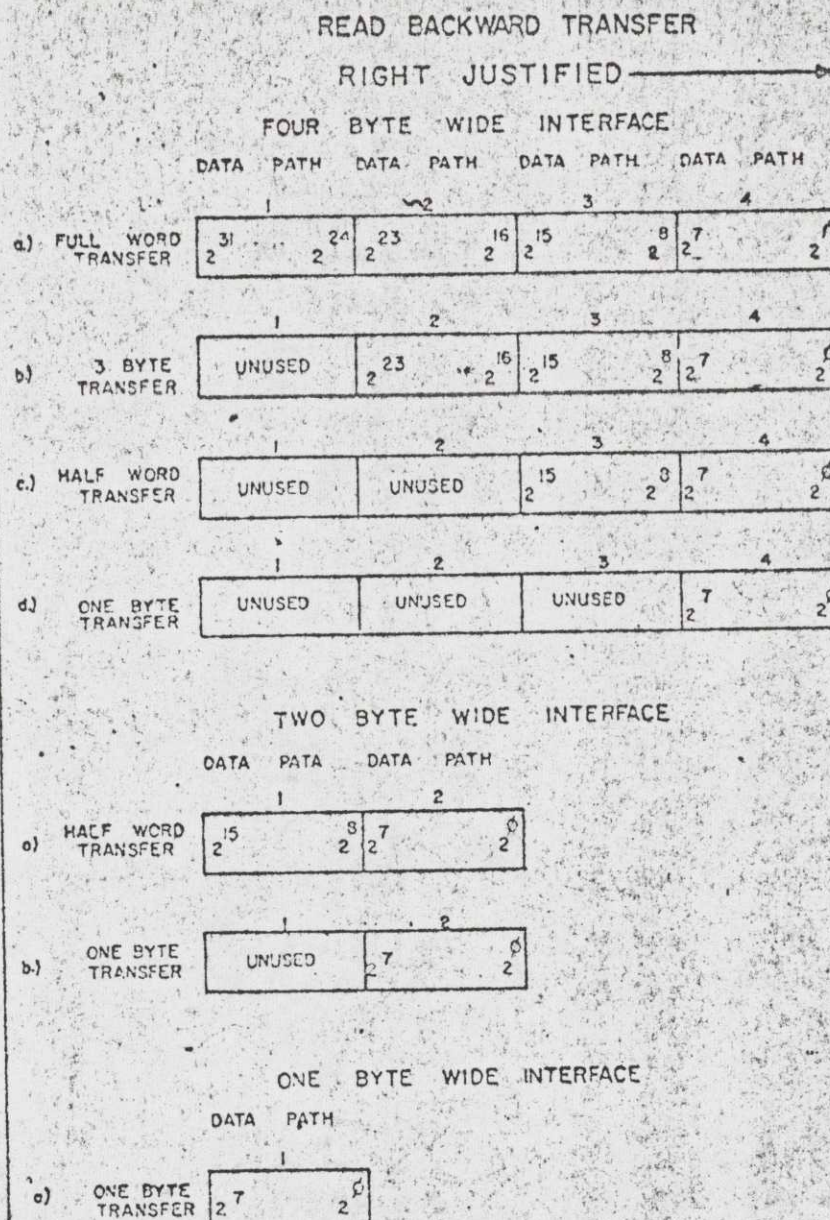
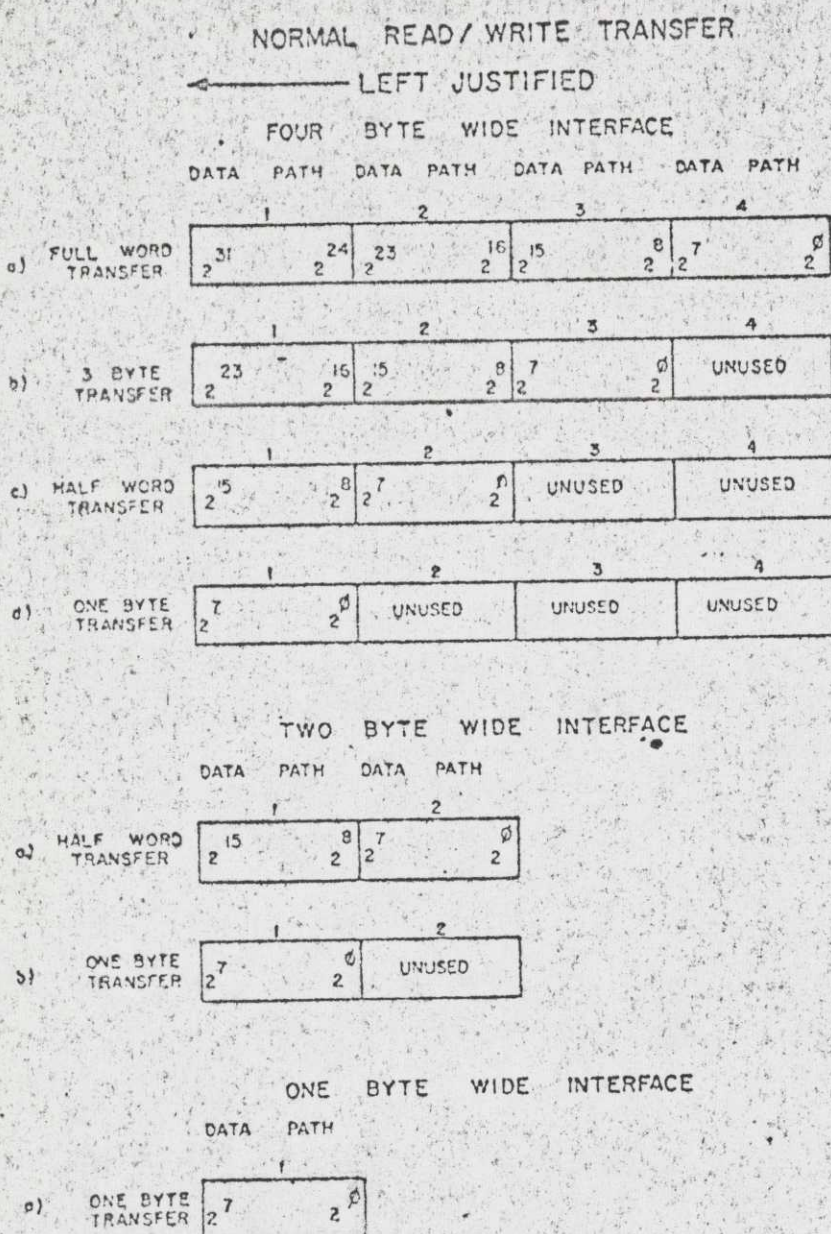


FIGURE 2.3.1 DATA FORMATS

(Reference Paragraph 2.3)

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2.4 (Continued)

Mnemonics for the lines are obtained by using the first or most significant letters in the words that name the lines, e.g., Service Code In (SCI), Terminate Out (TMO). The data lines, D, are followed by a digit indicating the data path (1 through 4), followed by another digit indicating the position of the line in the data path.

2.4.1 Data Path Lines (D 1-4, 0-7), Data Path Parity (D 1-4P)

Each set of Data Path lines is a one byte wide path (eight bits plus parity) that extends between the PCU and the IOC. The odd parity bits are separately generated for each byte of information.

Information transmitted on the data lines is arranged so the high order byte is placed on Data Path 1. Bit 0 is the high order bit and bit 7 is the low order bit on each Data Path. The parity bit is placed to the left of bit 0. Bits are always right justified on a byte basis if information less than eight bits wide is transmitted. Unused bits should be ZERO. Whenever more than one byte of information is transmitted, the bytes are not split in a field. The bytes are always together, either left or right justified, as determined by the CCE command code.

PCU's and IOC's of different path widths may be connected, as long as the wider path unit is aware that it is connected to a narrower path unit and tailors its dialog accordingly (see IOC and PCU Sub-system Specifications). Path width for any particular system is a static configuration and is determined at system installation time.

When transferring data on the two byte wide interface, a half word (two bytes) of data must be sent with each data transfer except for the last data transfer. When transferring data on the four byte wide interface, a full word of data must be sent with each data transfer except for the last data transfer. When a data transfer is suspended (to be resumed later), the last transfer before the suspension must utilize the full width of the interface.

The nature of the information on the data lines (data, service code, etc.) is determined by the dialog, according to the dialog syntax defined in Section 3.

Data is put on the data lines whenever the PCU/IOC raises STI/STO or TMI/TMO on a read/write operation. When, during a read/write operation, the IOC/PCU detects the fall of either STI/STO or TMI/TMO,

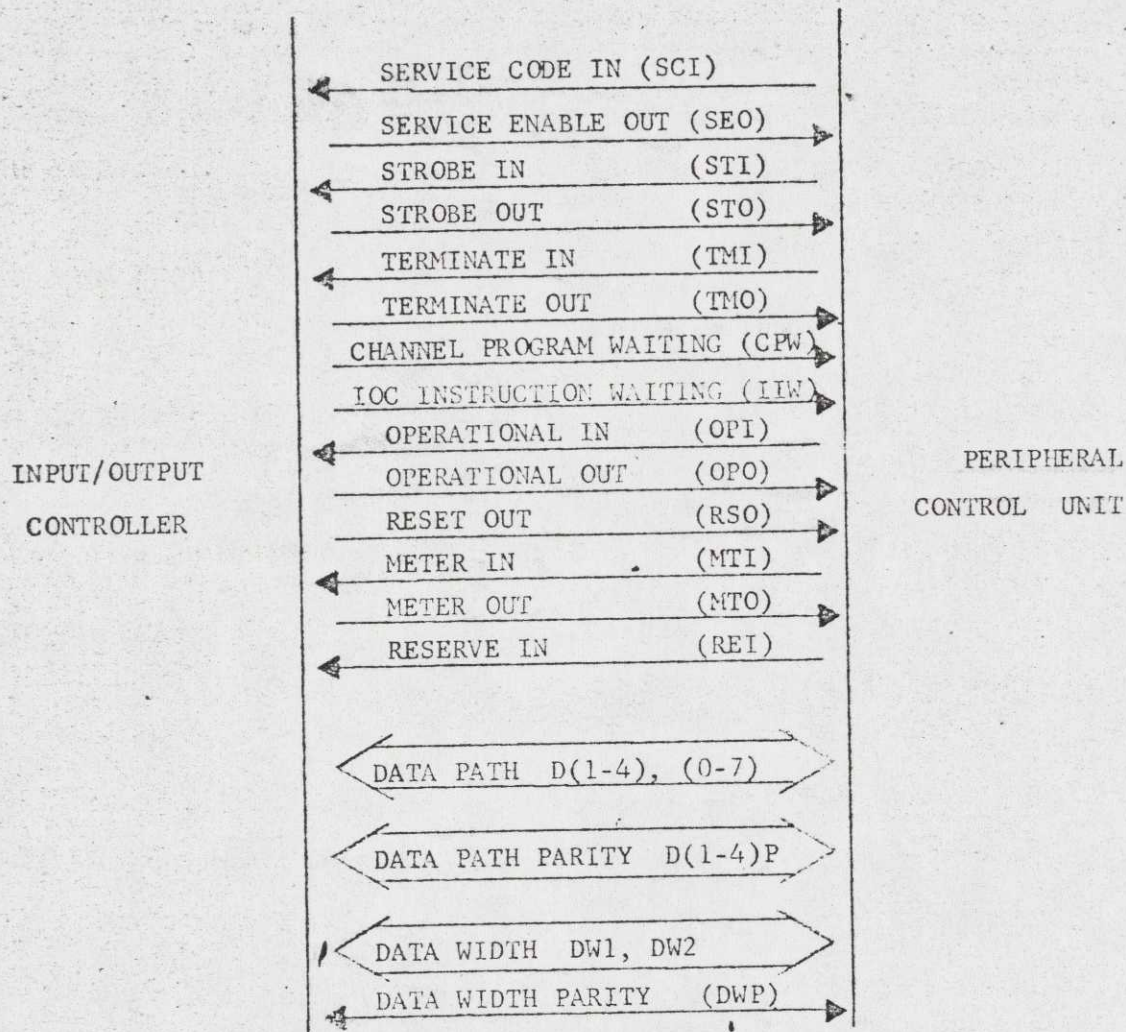


FIGURE 2.4.1 INTERFACE LINES
(Reference Paragraph 2.4)

DATA PATH WIDTH	NUMBER OF LINES
1	23
2	333
4	53

TABLE 2.4.1 NUMBER OF FUNCTIONAL INTERFACE LINES
(Reference Paragraph 2.4)

2.4.1 (Continued)

it should take the data from the data lines. The line drivers are enabled with the rise of the strobe signal for the first byte transferred. When not in use, the line drivers should be disabled. The line drivers should be disabled by the sending unit when it detects the fall of the receiving unit's strobe signal for the last byte transferred.

2.4.2 Data Width Lines (DW1, DW2) and Data Width Parity (DWP)

Data Width lines are bidirectional and are used only with multiple byte wide interfaces. These lines indicate which Data Paths are presently carrying data and which are presently unused. Only one Data Width line is defined for the two byte wide interface (DW1); two Data Width lines are defined for the four byte wide interface (DW1, DW2). There are no Data Width lines on the one byte wide interface. Table 2.4.2.1 shows the coding of these lines.

These lines follow the Data Path lines, i.e., the path width information is put on the Data Width lines at the same time the data is put on the Data Path lines, and is taken by the receiving unit at the same time. The Data Width drivers are enabled/disabled at the same time as the Data Path drivers.

Data Transfers (except for the last transfer) will utilize the full width of the interface and the Data Width lines should indicate this.

The Data Width Parity line (DWP) is bidirectional and is used as an odd parity line for the four byte wide interface Data Width lines. This line exists only on four byte wide PSI's. It will carry odd parity generated from the encoding of the Data Width lines. The Data Width Parity line follows the Data Width lines.

BYTES ON DATA LINES		DATA WIDTH IN CODING (LOGICAL STATE)	
TWO BYTE BUS	FOUR BYTE BUS	DW1	DW2
1 Byte	-----	ONE	---
2 Bytes	-----	ZERO	---
-----	1 Byte	ONE	ONE
-----	2 Bytes	ZERO	ONE
-----	3 Bytes	ONE	ZERO
-----	4 Bytes	ZERO	ZERO

TABLE 2.4.2.1 CODING OF DATA WIDTH LINES

2.4.3 Service Code In (SCI)

This line extends from the PCU to the IOC. When set, SCI indicates that the PCU has a service code sequence to send to the IOC. This line is fully interlocked with Service Enable Out (SEO). The PCU will not transfer the service code sequence until SEO is high. SCI may not rise unless SEO is low; SCI remains high for the duration of the service code sequence and will fall when the PCU detects the fall of STO/TMO for the last byte transferred in this service code sequence. SCI must fall after every service code sequence. If the PCU wants to send another service code sequence without any intervening data or command transfer, it must lower SCI until it detects the fall of SEO. Then it may again raise SCI and initiate the transfer of the next service code sequence.

The first byte transferred in a service code sequence is always a service code. (When not in use, this line must be reset to a logical ZERO state.)

2.4.4 Service Enable Out (SEO)

This line extends from the IOC to the PCU and is used to indicate that the IOC is ready to receive a service code sequence. This line is fully interlocked with Service Code In (SCI): SEO will only raise after SCI rises, and can only be reset when the IOC detects the fall of SCI. The fall of SEO enables the PCU to initiate a new operation over the PSI. A hardware failure will be assumed if this line is reset while SCI is high or set while SCI is low.

No dialog other than a PCU initiated service code sequence may take place over the interface unless both SCI and SEO are in a logical ZERO state. SEO cannot be raised if TMI/STI is high.

The IOC may use the high state of SEO to inhibit further action of the PCU until it (the IOC) has processed the service code and/or is ready to proceed with a read/write operation.

When not in use, SEO is reset to the logical ZERO state.

2.4.5 Strobe In (STI)

The Strobe In line, in conjunction with Strobe Out (STO), controls the data transfers on the interface. This line extends from the PCU to the IOC. It is activated by the PCU for a read or write operation.

2.4.5 (Continued)

For a read operation (data from PCU), the STI line can only be set if STO/TMO is reset (in the logical ZERO state). STI indicates to the IOC that data is present on the data lines. To obtain the data, the IOC responds with Strobe Out (STO) or Terminate Out (TMO), which resets STI in the PCU. When the IOC detects the fall of STI, it takes the data from the data lines. If necessary, the IOC can hold up the dialog at this point by delaying the resetting of STO (or TMO). Resetting STO signals the PCU that the data on the data lines can now be altered and that STI can be raised for another byte transfer dialog.

For a write operation, the roles of STO and STI are reversed. The IOC raises STO when it puts data on the data lines. When the PCU detects the rise of STO and it is ready to receive the data, it raises STI (or TMI). This causes the IOC to lower STO. When the PCU detects the fall of STO, it takes the data from the data lines. If necessary, the PCU may delay the dialog at this point by delaying the fall of STO (or TMI). When ready, the PCU resets STI (or TMI). This indicates to the IOC that it can now alter the data lines. STI cannot be reset before STO falls (for a write operation). STI may not be activated until data is present, as indicated by the STO line. The STO line may not be activated unless the STI line is reset. On both read and write operations, the PCU will use TMI instead of STI to terminate the current interface dialog.

STI must be reset to a logical ZERO state when not in use.

2.4.6 Strobe Out (STO)

The Strobe Out line is used by the IOC to indicate its participation in the dialog on the interface. This line extends from the IOC to the PCU.

For a read operation, STO is raised by the IOC when it detects the rise of STI or TMI and it is ready to obtain the data. On a read operation, STO cannot be raised if STI and TMI are both logical ZERO. When the PCU detects the rise of STO, it lowers STI (or TMI). Upon detecting the fall of STI (or TMI), the IOC takes the data from the data lines. If necessary, the IOC can hold up the dialog at this point of delaying the fall of STO. When it is ready to proceed, it lowers STO, indicating to the PCU that the data has been taken and that the data lines can now be altered. If the IOC terminates the current dialog, it will do so by raising TMO instead of STO for the last byte to be transferred.

2.4.6 (Continued)

For a write operation, the STO line indicates to the PCU that the IOC has data ready for it. The IOC puts the data on the data lines and raises STO. The STO line may not be activated for a write operation unless the STI and TMI lines are reset. The STO line must be reset when STI/TMI is activated. When the PCU detects the fall of STO, it may then take the data. If necessary, the PCU can hold up the dialog at this point by delaying the lowering of STI (or TMI). When ready, the PCU lowers STI (or TMI) indicating to the IOC that the data lines can now be altered.

This line must be reset to a logical ZERO state when not in use.

2.4.7 Terminate Out (TMO)

Terminate Out is used by the IOC to end the current dialog, whether read or write. The TMO line extends from the IOC to the PCU.

The rules for the rise and fall of TMO are the same as those for STO. The same comments apply. However, the meaning of TMO is different from that of STO, as indicated below.

- For a write operation, TMO can indicate one of the following conditions:

- A) For a data transfer, TMO implies that a byte being transferred is the last byte of a field and the data count is exhausted. Since data chaining is transparent to the PCU, TMO rises only when the count of the last data chained DCW in the data chain array is exhausted. Due to an error, the transfer may be terminated prematurely.
- B) For a command or IOC instruction transfer, TMO indicates that the transfer is complete with the byte(s) being sent on the current transfer and that no more bytes are forthcoming.

During a write operation, TMO can only rise if STI and TMI are low, and will fall when the IOC detects the rise of STI/TMI.

For a read operation, TMO is used to indicate one of the following conditions:

- A) In a data transfer, TMO indicates that the byte(s) being transferred or a previous byte has exhausted the data count. All bytes following the byte that exhausted the count are discarded. Since data chaining is transparent to the PCU, TMO will only rise when the count associated with the last data chained DCW of the data chain array is exhausted. Due to an error, the transfer may be terminated prematurely.

2.4.7 (Continued)

- B) In a service code sequence, TMO will be used to indicate the following:

The IOC wants the PCU to stop the transfer of the sequence immediately. An error during the sequence is conveyed by the IIW line.

In a read operation, TMO will indicate one of the above conditions by being sent instead of STO. During a read operation, TMO can only rise if STI/TMI is high, and will fall when STI/TMI falls.

This line must be reset to a logical ZERO state when not in use.

2.4.8 Terminate In (TMI)

Terminate In is used by the PCU to end the current dialog, whether read or write. The TMI line extends from the PCU to the IOC. The rules governing the rise and fall of TMI are the same as for STI. The same comments apply; however, the meaning of TMI is different from that of STI, as indicated below.

For a write operation, TMI is sent instead of STI and can indicate one of the following conditions:

- A) For a data transfer, TMI indicates that the byte(s) being received is (are) the last byte(s) the PCU will accept for this transfer sequence (e.g., media is exhausted), or that the PCU is temporarily suspending the data transfer sequence.
- B) For a command transfer, TMI indicates that the byte(s) being received is (are) the last byte(s) required by the PCU.

For a read operation, TMI is sent instead of STI and indicates one of the following conditions:

- A) For a data transfer, TMI indicates that the byte(s) being transferred is (are) the last byte(s) available from the media for this data transfer sequence, or that the PCU is temporarily suspending the data transfer sequence. The suspended sequence may be resumed by using the appropriate service code. However, it is important to note that some applications of this interface may not allow suspend operations.

2.4.8 (Continued) -

- B) For a service code sequence, TMI indicates that the byte(s) being transferred is the last byte(s) in the service code sequence.

TMI must be set to logical ZERO when not in use.

2.4.9 Channel Program Waiting (CPW)

Channel Program Waiting indicates to the PCU that a channel program (DCW list) is waiting. The CPW line extends from the IOC to the PCU.

A command received by the IOC results in the IOC setting the CPW line to a logical ONE state. As soon as the PCU is able, it issues an Initiate New Program service code to start the new channel program, and the IOC then begins transferring a logical channel number and the first DCW to the PCU. CPW remains up until no new channel programs remain to be initiated. CPW resets for the last entry in the initiation queue when STO resets for the transmission of the Initiate New Program service code from the PCU to the IOC. The CPW line is reset to a logical ZERO when not in use.

2.4.10 IOC Instruction Waiting (IIW)

IIW indicates to the PCU that the IOC has an instruction to send. The IIW line extends from the IOC to the PCU. The PCU should, upon recognizing that IIW is high, send an Initiate IOC Instruction service code to the IOC at its next service code sequence opportunity. The IOC then sends the IOC Instruction to the PCU, accompanied by a logical channel number, if applicable.

If a data transfer is in progress at the time IIW rises, it should continue to its normal termination point. If, however, the IOC requires immediate transmission of an IOC Instruction, it will terminate data transfer by sending TMO instead of STO.

If IIW and CPW are up at the same time, the PCU should service IIW first.

When IIW is high, the PCU should service it before any other service code sequences it wishes to send.

IIW will reset when STO resets for the transmission of the Initiate IOC Instruction service code (or whatever service code is used to accomplish this action). If the IIW line is active at the end of a Service Code sequence, the PCU is to assume that any transfers called for by the service code will not occur. The IIW line is reset to a logical ZERO state when not in use.

2.4.11 Operational Out (OPO)

Operational Out indicates the state of the IOC. When activated, it indicates that the IOC is operational and capable of communication with the PCU. When deactivated, it means that the IOC is powered down or is in a state that makes it incapable of responding on the PSI. The OPO line extends from the IOC to the PCU.

When the PSI is physically disconnected from the IOC, this line is deactivated. This line may be activated or deactivated at any time. If this line is deactivated while dialog is in progress, the PCU ceases the dialog on the PSI. If OPO is down, the PCU should not attempt any dialogs on the PSI. See IOC Subsystem specifications for conditions relating to the state of this line.

2.4.12 Operational In (OPI)

Operational In indicates the PCU operational state to the IOC. The OPI line extends from the PCU to the IOC.

When activated, OPI indicates that the PCU is operational and capable of communication with the IOC. When deactivated, it means that the PCU is powered down or is in a state that makes it incapable of responding on the PSI. See PCU subsystem specifications for conditions relating to the state of this line.

The Operational In line will be deactivated if it is set when the IOC activates the Reset Out (RSO) line. The OPI line will remain deactivated until resetting (initialization) and any self diagnosis activities intrinsic to initialization are completed.

When the PSI is physically disconnected from the PCU, this line is deactivated. This line may be activated or deactivated at any time (except it may not be activated if RSO is high). If it is deactivated while some dialog is in progress on the interface, the IOC will cease the dialog on the PSI.

2.4.13 Reset Out (RSO)

The Reset Out line extends from the IOC to the PCU. Reset Out resets and initializes the PCU to a known state. Device adapters and devices may also be reset and initialized to a known state as a result of this line being activated (see unit specifications). For a shared PCU (more than one PSI to a PCU), the rise of RSO on one of the PSI's may not reset the entire PCU (see unit specifications). The RSO line is implemented as a pulse of ten microseconds minimum duration. When RSO is raised, the affected unit(s) will immediately cease dialogs on the PSI.

2.4.13 (Continued)

While initialization is taking place in the PCU, the OPI line will be in the logical ZERO state. When initialization is complete and RSO has dropped, OPI can be raised to logical ONE.

When not in use, this line is to be reset to the logical ZERO state. Note that RSO may rise independently of the state of OPI.

2.4.14 Meter Out (MTO)

Meter Out is a line from the IOC to the PCU used to condition all elapsed time (usage) meters in the attached PCU and peripheral devices. For the 6000 Line, Meter Out is high when the IOC Power On meter is recording time. This line must be reset to a logical ZERO state when not in use.

2.4.15 Meter In (MTI)

Meter In is a line from the PCU used to indicate that billing conditions have been met in the device and that device end has not yet been reached (see subsystem specifications).

The state of the Meter In line may affect the STOP sequence in the CPU (see CPU specifications).

Meter In will not be high in the following cases:

- A) Between the time a device finishes the execution of a command and the time the IOC accepts the termination message.
- B) Between the time a device finishes the execution of a command and the time the PCU accepts the next command for the logical channel during command chaining.
- C) While the device is awaiting initiation of an automatic start, such as a communications unit awaiting for an external signal when in the Prepare to Receive mode.

Meter In and Meter Out will exist in all NPL peripheral subsystems. This line must be reset to a logical ZERO state when not in use.

2.4.16 Reserve In (REI)

Reserve In is a line from the PCU and is available to condition PSI switching. Reserve In is used by free-standing switches located between the PCU and the IOC to condition switching operations. The path between the PCU and the IOC cannot be severed when REI is high.

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2.4.16 (Continued)

When in the logical ZERO state, REI indicates that the PCU no longer requires use of the currently established communications path, and that switching the PSI is therefore, allowed.

REI is high whenever:

- A) A channel program is active in the PCU; i.e., from the time the PCU sends the Initiate New Program service code until the termination message is sent for that channel program.
- B) A logical channel on this peripheral subsystem has been previously seized by a Seize command, and has not yet been released.

When not in use, this line must be reset to a logical ZERO state.

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3.0 SERVICE CODES

This interface uses the concept of service codes to pass control information. The content or meaning of the service code is transparent as far as the dialog on the interface is concerned. It has meaning to the parties on either end of the interface. Therefore, just because equipment is connected with the PSI interface, does not constitute complete compatibility. The content of the dialog must be understood by both parties on the interface to achieve compatible operation. Although this interface is used on NPL equipment and 6000 equipment, different service codes are used. The service codes used with the IOM are described in the document EPS-1, 655 IOM Peripheral Subsystem Interface Adapter, #43A177880.

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4.0 INTERFACE DIALOG AND SEQUENCES

4.1 General

This section discusses interface dialogs. Considerations that affect the entire interface (as opposed to those that affect only one or a few lines) are discussed.

4.2 Data Throughput

Data throughput on the interface is inversely proportional to the cable length used, and significantly affected by the turn-around time of each party on the interface. Cable propagation delay is important because of the interlocked nature of the signals on the interface. Table 4.2 lists representative data transfer rates for different path widths at different cable lengths. Circuit delays are representative worst-case conditions for NPL custom fast circuits, and for a combination of flat cable and coaxial cable.

TABLE 4.2 REPRESENTATIVE PSI DATA RATES

CABLE LENGTH (FEET)	25	50	75	100	125
One byte wide, data rate (megabytes/second)	2.94	2.00	1.51	1.22	1.02
Two bytes wide, data rate (megabytes/second)	5.88	4.00	3.03	2.44	2.04
Four bytes wide, data rate (megabytes/second)	11.75	8.00	6.07	4.88	4.08

These transfer rates were calculated using the following technique:

- A) The fully interlocked transfer technique specified in the document requires four signal traversals of the bus plus associated turn-around delay in each unit.
- B) Assuming that the receiver is gated directly into the driver,

4.2 (Continued)

the time for one bus traversal (T_D) is:

$$T_D = t_d + t_r + t_c (L)$$

where:

t_d = driver delay (time)

t_r = receiver delay (time)

t_c = cable delay (time/foot)

L = cable length (feet)

This method does not allow for backup logic or synchronization time in the associated control units.

C) The time for each information transfer is:

$$4T_D = 4 [t_d + t_r + t_c (L)]$$

D) The rate of information transfer is:

where: $N/4T_D$
 N = number of bytes per transfer.

E) The rates in Table 4.2 were calculated using the following figures:

t_d = 20 nanoseconds (maximum)

t_r = 25 nanoseconds (maximum)

t_c = 1.6 nanoseconds/foot (maximum)

4.3 Parity and Data Integrity

Odd parity is carried on all interface data lines. Each eight bit byte has its own parity bit. The lines used to control the data flow (STI, STO, SCI, SEO, etc.) have no parity check associated. However, the control lines are interlocked to ensure dialog integrity on the interface.

For data transmission on the interface, each byte must have the correct odd parity generated for the bit pattern. This is the responsibility of the transmitting party. The receiving party is to verify the transmission by recalculating the parity and comparing it with the transmitted parity. If the comparison is not valid, a transmission error is assumed.

4.3 (Continued)

- A) When the PCU detects a parity error on a logical channel number, it may abort the interface by lowering OPI.
- B) When detecting a parity error on a service code sequence, the IOC will terminate the service code sequence and notify the PCU by sending it an IOC Instruction. When a parity error occurs in a service code sequence, IIW must be raised before the IOC drops its strobe signal with the last transfer.
- C) When a parity error is detected during data transmission, the transmission will continue until the end. If the error was detected by the PCU (write operation), it can retry the transmission by using the Move Pointer service code. This also applies in the case of parity errors on DCW transfer (from IOC to PCU). The IOC, upon detecting a parity error, on data transmission (read), will notify the PCU (for a possible retry) by raising IIW before dropping STO/TMO for the last byte transferred and subsequently sending the appropriate IOC Instruction.
- D) When a parity error occurs on an IOC Instruction, the PCU may abort the interface by lowering OPI.

4.4 Signal Interlocks

All interface control signals are implemented as levels rather than pulses, except for RSO. The signals are implemented in a manner that requires each party to consider the state of the other party's lines before changing its own. Therefore, a faster party must wait for the slower one; two fast parties may run the interface at maximum speed. This enables a wide variety of equipment to use this interface with no timing adjustments.

The interlock scheme on the PSI is self-adjusting for cable length. There are no skew timing restrictions. For short cables, the interlock time is shorter, but adequate for skew considerations. There is a minimum cable length, depending on circuits used. As the cable gets longer, the interlock and data settling time is proportionately longer.

4.5 Time Outs - Response Time Consideration

If for some reason a dialog stops on the interface, it is detected in one of two ways. If a time dependent device is running, a data overrun results in the peripheral subsystem and the operation is

4.5 (Continued)

terminated. If the dialog does not involve any time dependence, no data overrun occurs and software supported system time-outs are relied upon to detect the cessation of interface dialog activity.

4.6 Signal Dialog

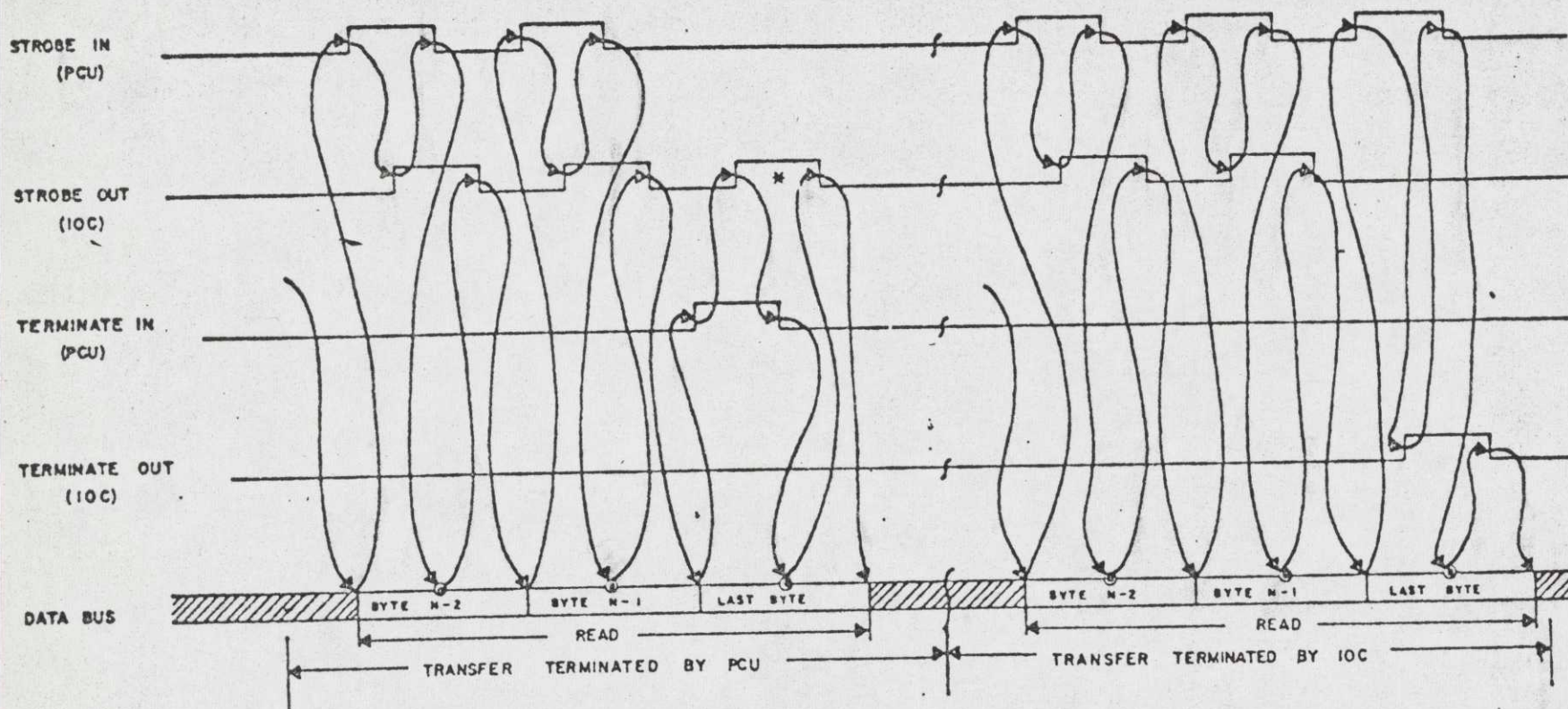
All dialog on the interface consists of a combination of read and write operations.

4.6.1 Read Operation

Figure 4.6.1-A shows a signal dialog for a read operation on the interface. Each signal transition is shown as seen at the source. The sequence starts with the placing of the data on the data bus and the raising of Strobe In (STI). The IOC is thus enabled to raise STO when it is ready to receive the data. The STO signal propagates to the PCU and enables the resetting of STI. The resetting of STI propagates to the IOC. Sufficient time has passed for the data to be settled at the receivers, and it may be taken at this time. When the IOC drops STO, it is an indication to the PCU that the data has been received and that the data bus can now be changed and the next transfer started. If this was the last transfer in the sequence, the PCU must disable its drivers when it detects the fall of STO/TMO.

If the sequence is a PCU service code sequence (see Figure 4.6.1-B), the PCU will initiate activity by raising Service Code In (SCI). The IOC will answer by raising Service Enable Out (SEO). When the PCU detects the rise of SEO, it can put the data on the Data lines and raise STI as described above.

The read operation may be terminated either by the IOC or the PCU. The IOC can terminate it on a transfer by answering with TMO instead of STO. The PCU can terminate it by sending TMI on a transfer instead of STI. If the sequence to be terminated is a service code sequence, the PCU will send TMI instead of STI for the last transfer. The IOC will answer (as usual) with STO. When the PCU detects the fall of STO it can then lower SCI, which in turn will cause SEO to fall. Once SEO is down, the IOC or PCU is free to start an information transfer (e.g., data, status, command) if it was specified by the service code. However, once SCI is lowered, no dialog may take place until SEO is lowered by the IOC.



* THE IOC MAY RESPOND WITH EITHER (STO) OR (TMO) BUT NOT BOTH.

FIGURE 4.6.1-A READ OPERATION SIGNAL DIALOG

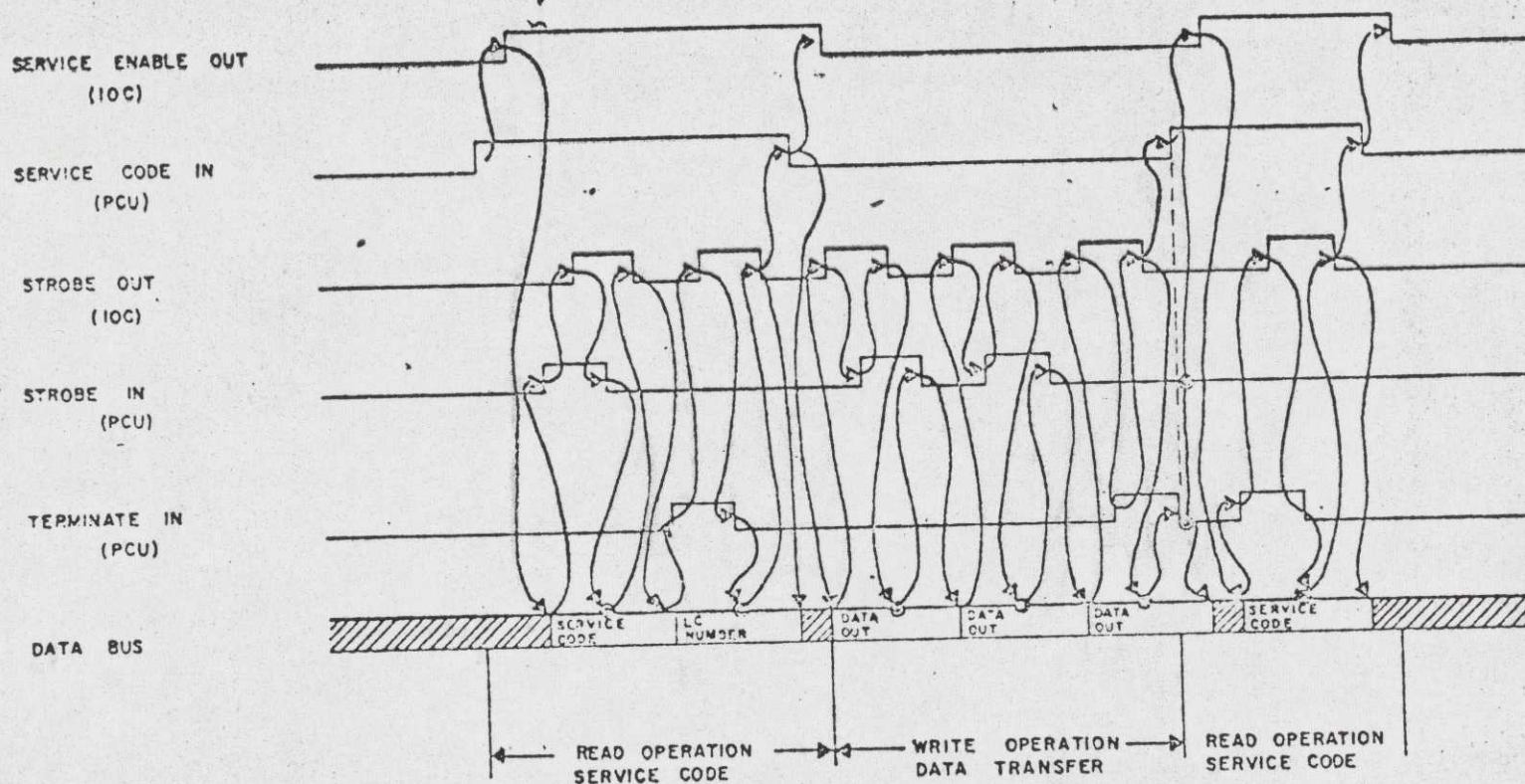


FIGURE 4.6.1-B TRANSFER CONTROL

4.6.2 Write Operation

Figure 4.6.2 shows a signal dialog for a write operation on the interface. Each signal transition is shown as seen at the source. The sequence was previously started by the PCU sending a service code to the IOC. The IOC, after noting the fall of SCI, drops SEO and, when ready, places the data on the Data lines and raises STO. The data and STO propagate to the PCU and enable it to raise STI when it is ready to take the data. When STI propagates to the IOC, the IOC lowers STO. The resetting of STO propagates to the PCU. Sufficient time has passed for the data to be settled at the receiver, and it may be taken at this time. When the PCU drops STI, it is an indication to the IOC that the data has been received and that the Data lines can now be changed and the next transfer started. If this was the last transfer in the sequence, the IOC must disable its drivers when it detects the fall of STI/TMI.

The sequence may be terminated either by the IOC to the PCU. The IOC can terminate it by sending TMO instead of STO with the last transfer. The PCU can terminate the sequence by answering the STO signal for the transfer with TMI instead of STI.

4.7 Transfer Control

Figure 4.6.1-B illustrates transfer control techniques for a typical interface dialog (read to write, write to read). Where the IOC terminates a read operation, it will not initiate a write operation. The PCU may not initiate a read data operation after a write operation. It may, however, initiate a service code sequence, which is a read operation. In the case where the IOC has terminated the write operation, the PCU may not raise the SCI line until the STI/TMI line is reset. If the PCU has terminated the write operation, it may raise the SCI line at any time after or when the TMI line falls. Following a service code sequence and the lowering of SCI, no dialog may take place on the interface until SEO is lowered by the IOC. To ensure proper turnaround of the bidirectional data path, the sending unit must disable its drivers when it detects the fall of the receiving unit's strobe signal for the last transfer.

4.8 IOC Instruction Sequence

When the IOC has an instruction to send to the PCU, it will raise IIW. If a dialog is in progress at this time, and the IOC cannot wait until it is completed, the IOC will terminate it by sending TMO instead of STO in a byte transfer; otherwise, the dialog will proceed to its normal termination. The PCU will then send an

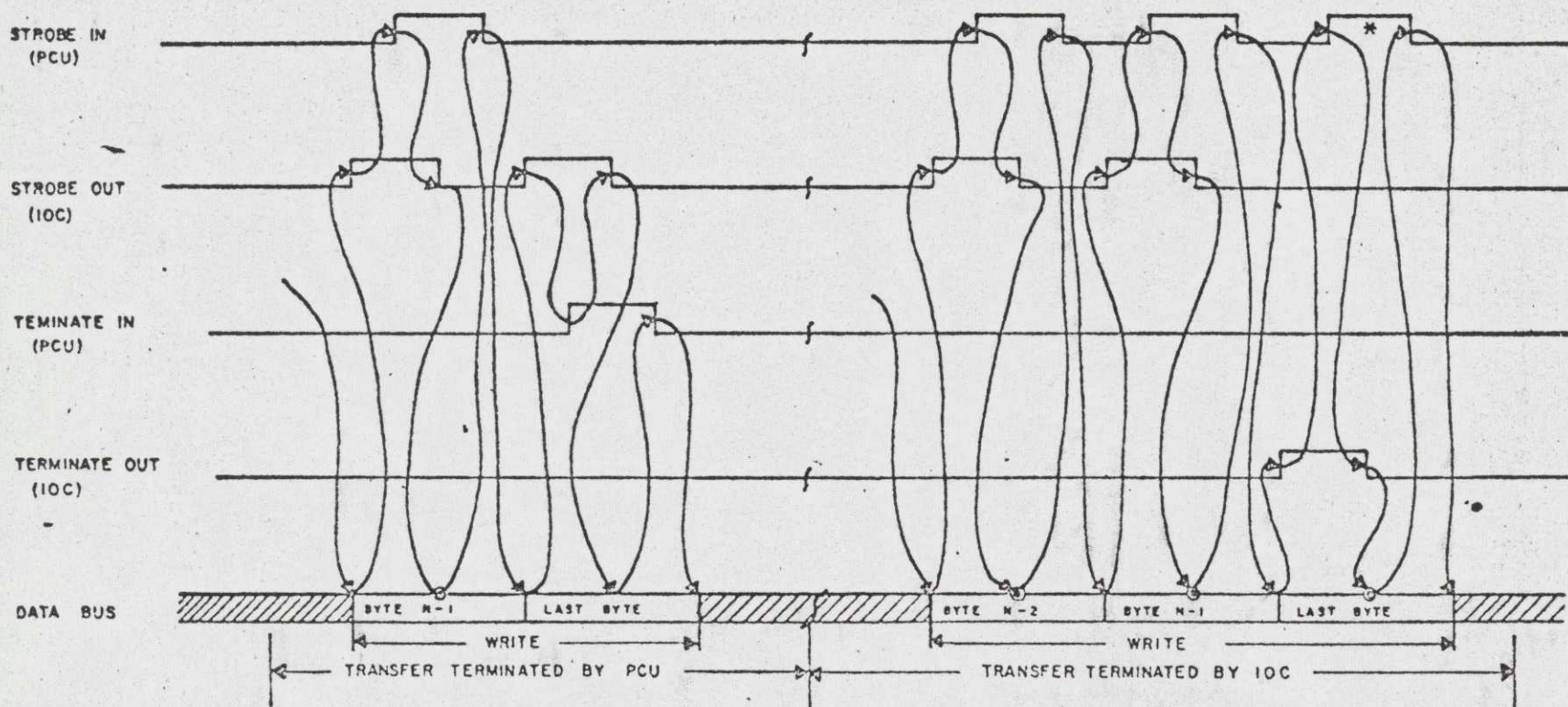


FIGURE 4.6.2 WRITE OPERATION SIGNAL DIALOG

4.8 (Continued)

Initiate IOC Instruction service code to IOC. If this is the last or only IOC Instruction to be sent, the IOC will lower IIW together with STO upon the receipt of the Initiate IOC Instruction service code (or whatever service code is used to accomplish this action). The IOC will then send its instruction to the PCU with or without a logical channel number. On one byte wide interfaces, the logical channel number, if sent, will be sent as the first transfer followed by the IOC Instruction. On multiple byte wide interfaces, the two may be sent simultaneously, the logical channel number on Data Path 1 and the IOC Instruction on Data Path 2.

4.9 Length Checking (Not presently utilized on the 6000 Line)

Data transfer length checking is performed by the PCU. In cases where unequal length is detected, the PCU may or may not report it to the IOC depending on whether or not the Unequal Length Check flag is set in the IDCW that called for the data transfer. Unequal length is reported in the PCU/device status.

For length checking, the PCU will get the data count from the data transfer DCW. In data chaining operations, a count representing the total count for the DCW chain will be available to the PCU in a DCW immediately preceeding the data chain. In either case, the PCU will compare this count against the media length. If not equal, an unequal length indication will be noted in the PCU/device status, provided the data transfer DCW requested unequal length checking in its flags field.

4.10 Bootload In (Initial Program Loading)

Bootload In is the process of loading main memory with the information necessary to initiate processing when the contents of main memory are not suitable for processing.

The Bootload sequence on the PSI will appear as a normal channel program execution and termination.

4.11 Sequence Restrictions

Service codes transferred over the interface may occur in any order. Each channel program in operation may be at any state of completion, and each service code transferred may be for a different logical channel. The only restrictions on the sequence of service codes are practical ones:

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4.11 (Continued)

- A) A service code may not be issued for an inactive channel (except for Attention or Special type interrupts). If this restriction is violated, the IOC will raise IIW and subsequently send an IOC Instruction notifying the PCU of the error.
- B) A Termination or Interrupt service code, when called for by the IDCW, will follow execution of the command and/or data transfer, not precede them.
- C) Certain subsystems may have restrictions on service code sequences. See subsystem specifications for any such restrictions.

5.0 PHYSICAL ASPECTS OF PSI

The physical aspects of the PSI consist of the circuits, electrical considerations, cables and connectors.

5.1 Recommended Circuits

This specification assumes the implementation of this interface with the following circuits, shown in Figures 5.1-A through 5.1-E.

5.2 Cable Lengths

The maximum cable length is 140 feet and the minimum is 12 feet.

5.3 Power Control Affects on Signals

When the power in each system is brought up, the Operational lines are not to be activated until all transients have settled. Also, when power goes down, an attempt should be made to deactivate the Operational line before the low voltage affects the circuits operation.

5.4 Connectors

The connectors to be used on this interface have not yet been defined. Since this is a star interface, a separate cable is used to connect to each IOC/PCU pair.

5.5 Cables

The cable to be used is $\leq 85 \Omega$ coax. The transmitters are terminated (shunt termination) with 85Ω to ground.

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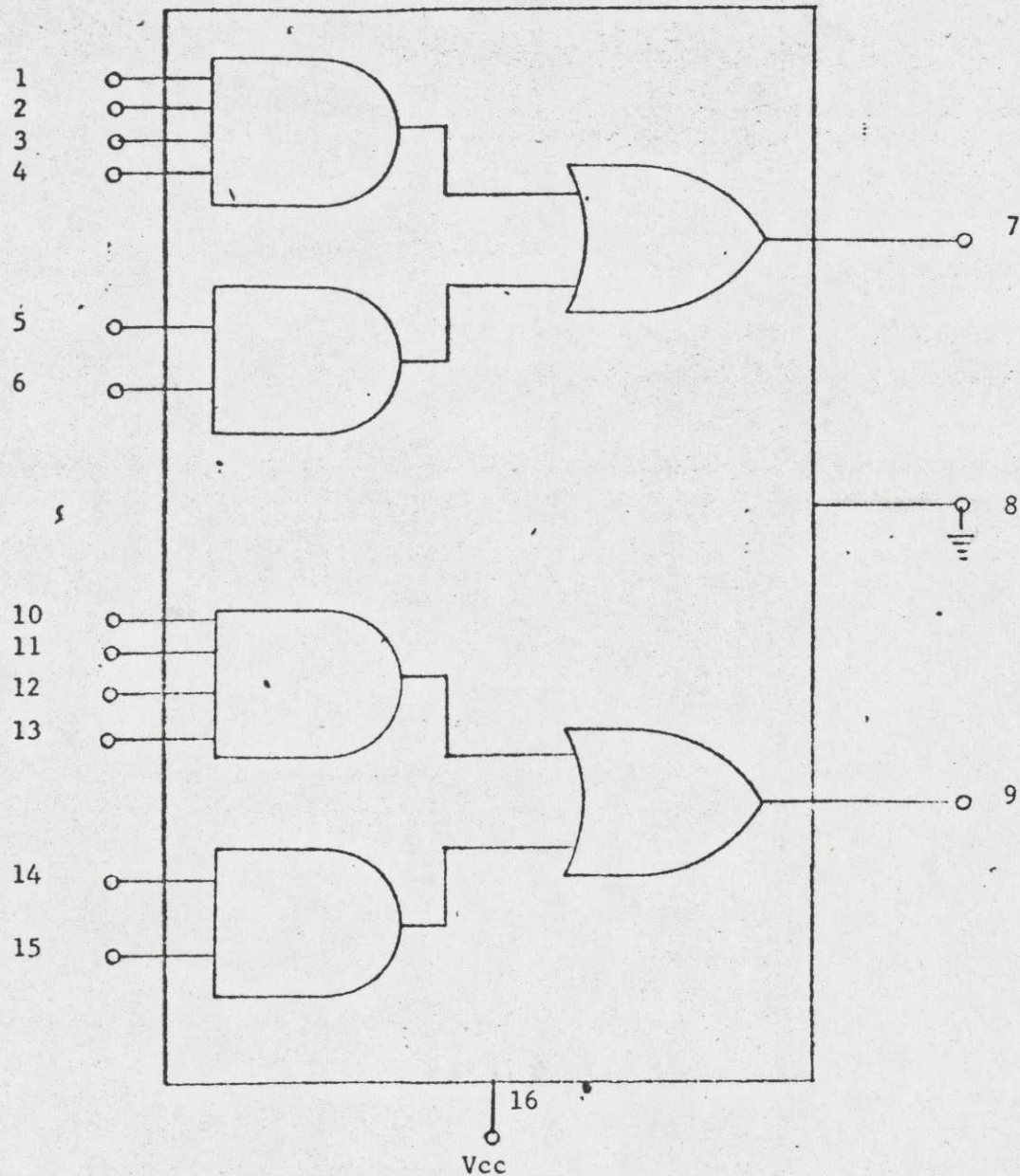
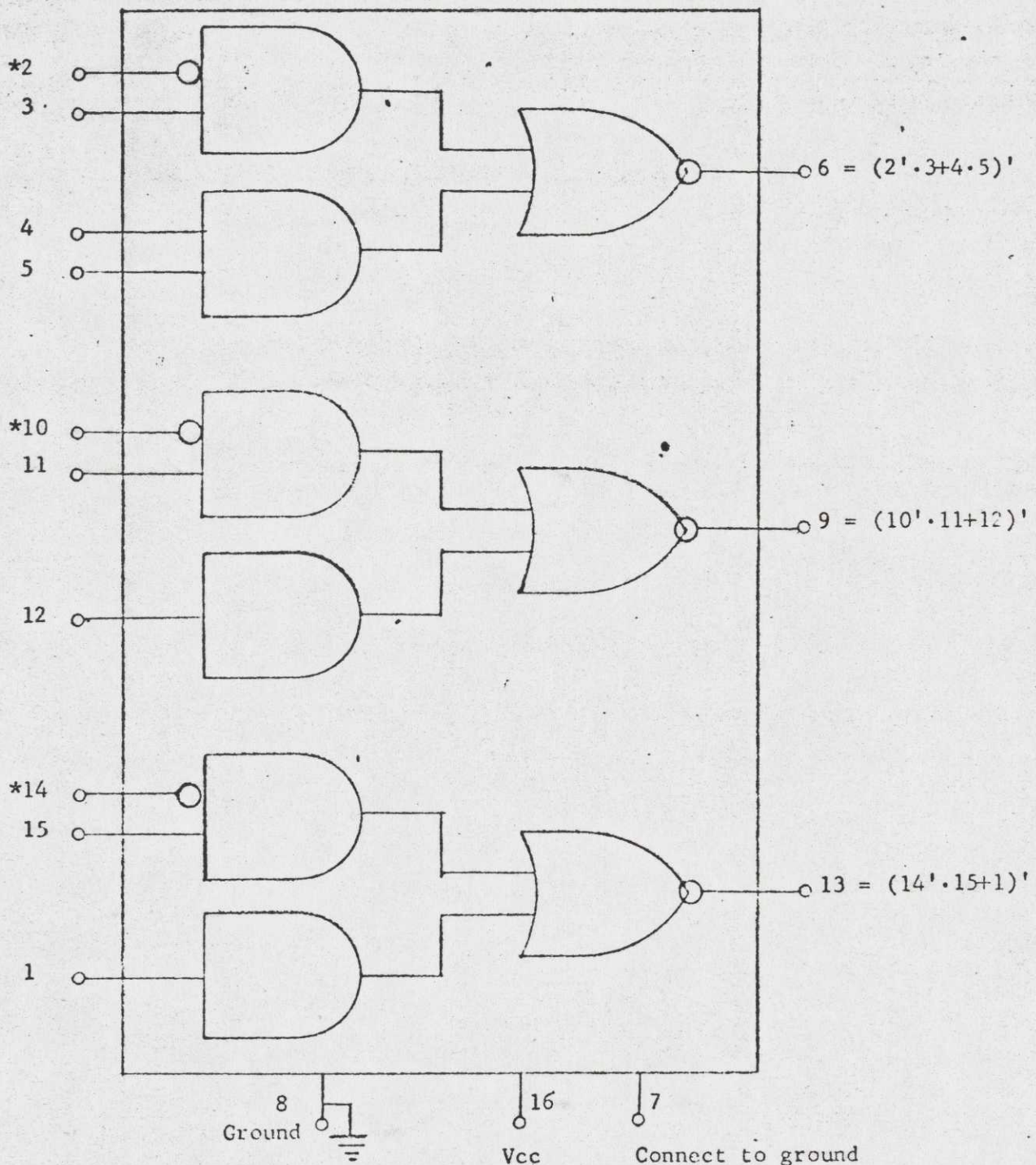


FIGURE 5.1-A PSI CIRCUITS, DKLD1 DRIVER



*Transmitters are connected to these pins.

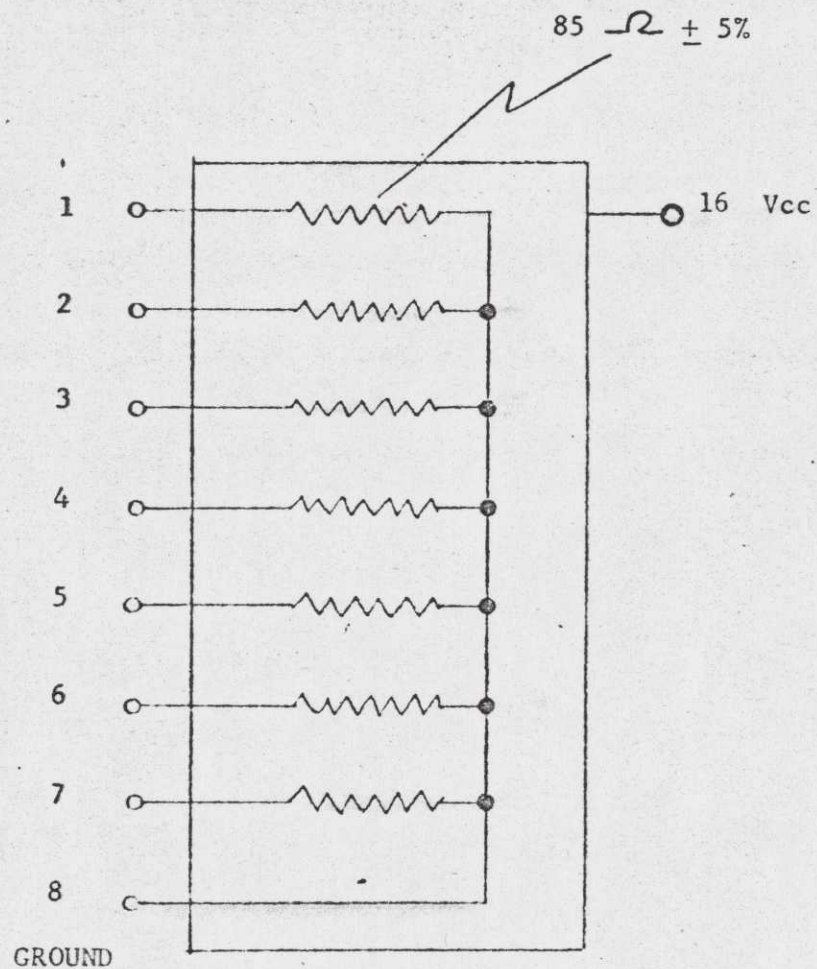
FIGURE 5.1-B PSI CIRCUITS, DKLRI RECEIVER

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Pins 9, 10, 11, 12, 13, 14 have no connection.

FIGURE 5.1-C PSI CIRCUITS, TERMINATION

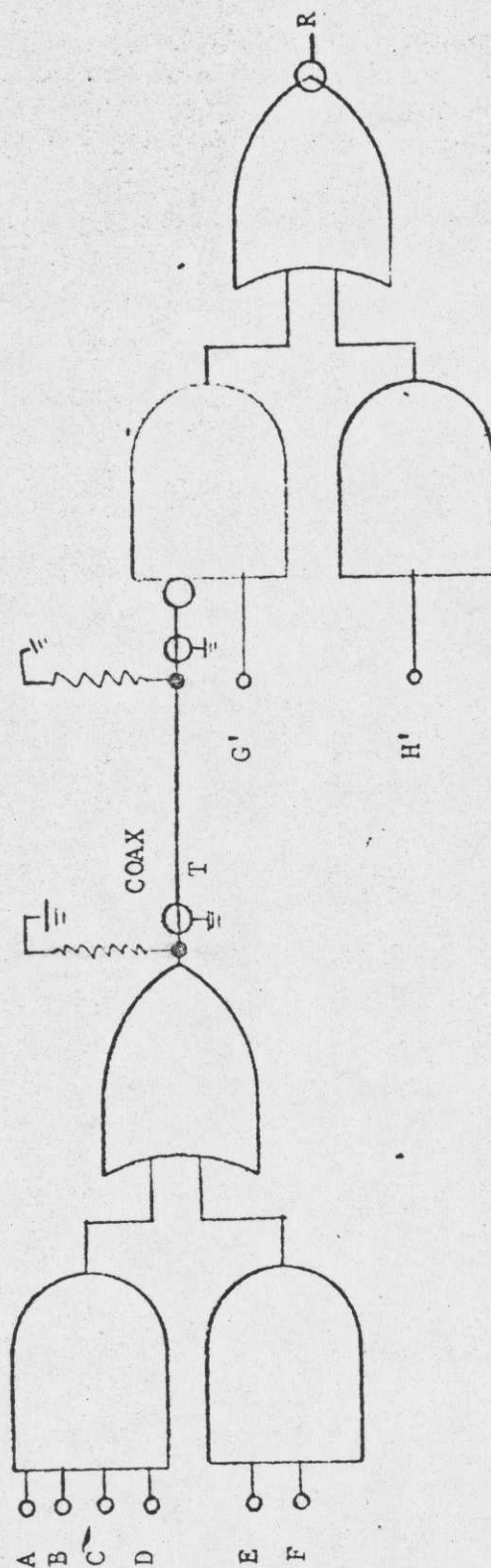
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$$R = (A \cdot B \cdot C \cdot D + E \cdot F + G) \cdot H$$

FIGURE 5.1-D PSI CIRCUITS, RECOMMENDED IMPLEMENTATION

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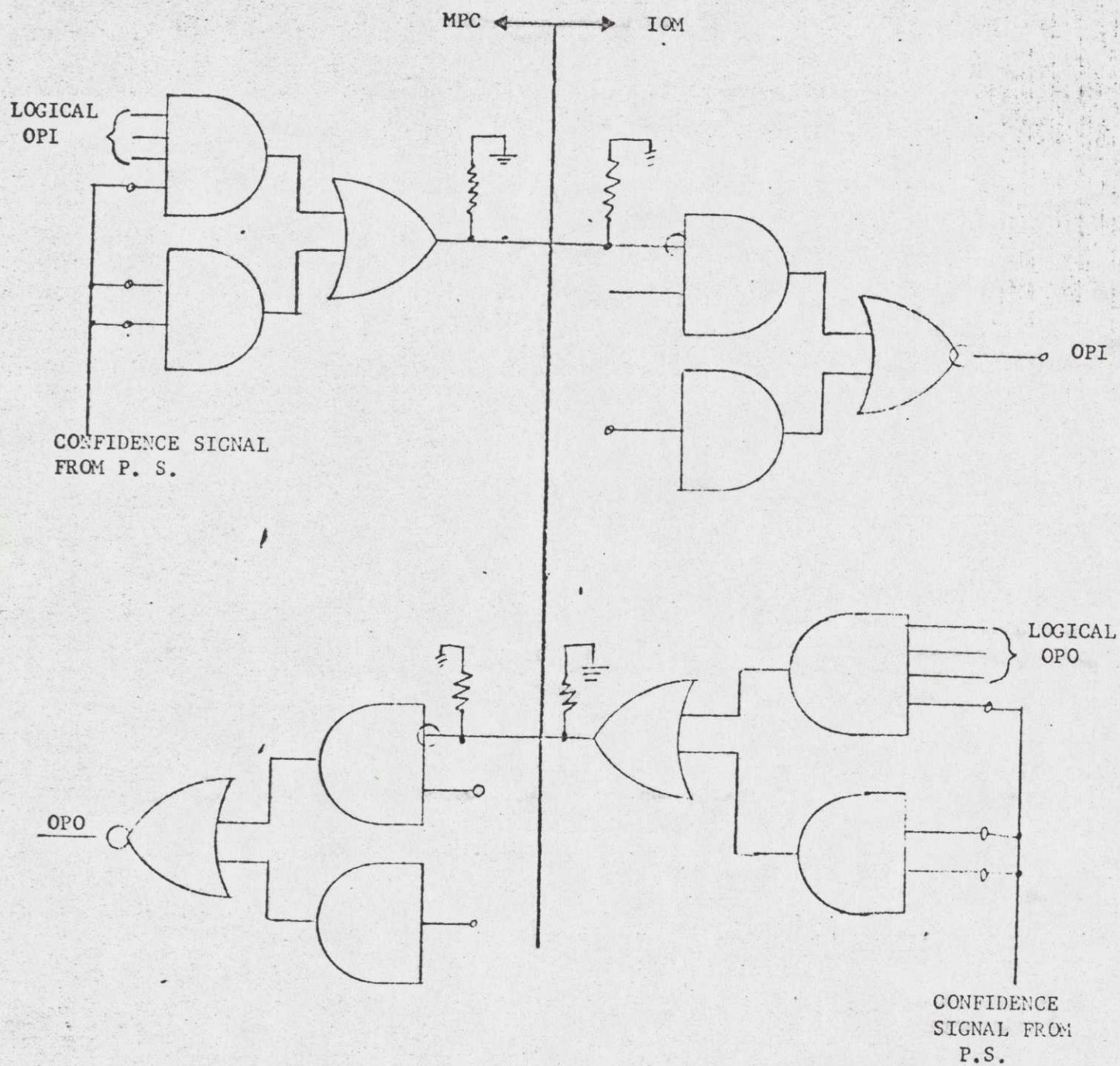


FIGURE 5.1-E PSI CIRCUITS, OPI/OPO IMPLEMENTATION

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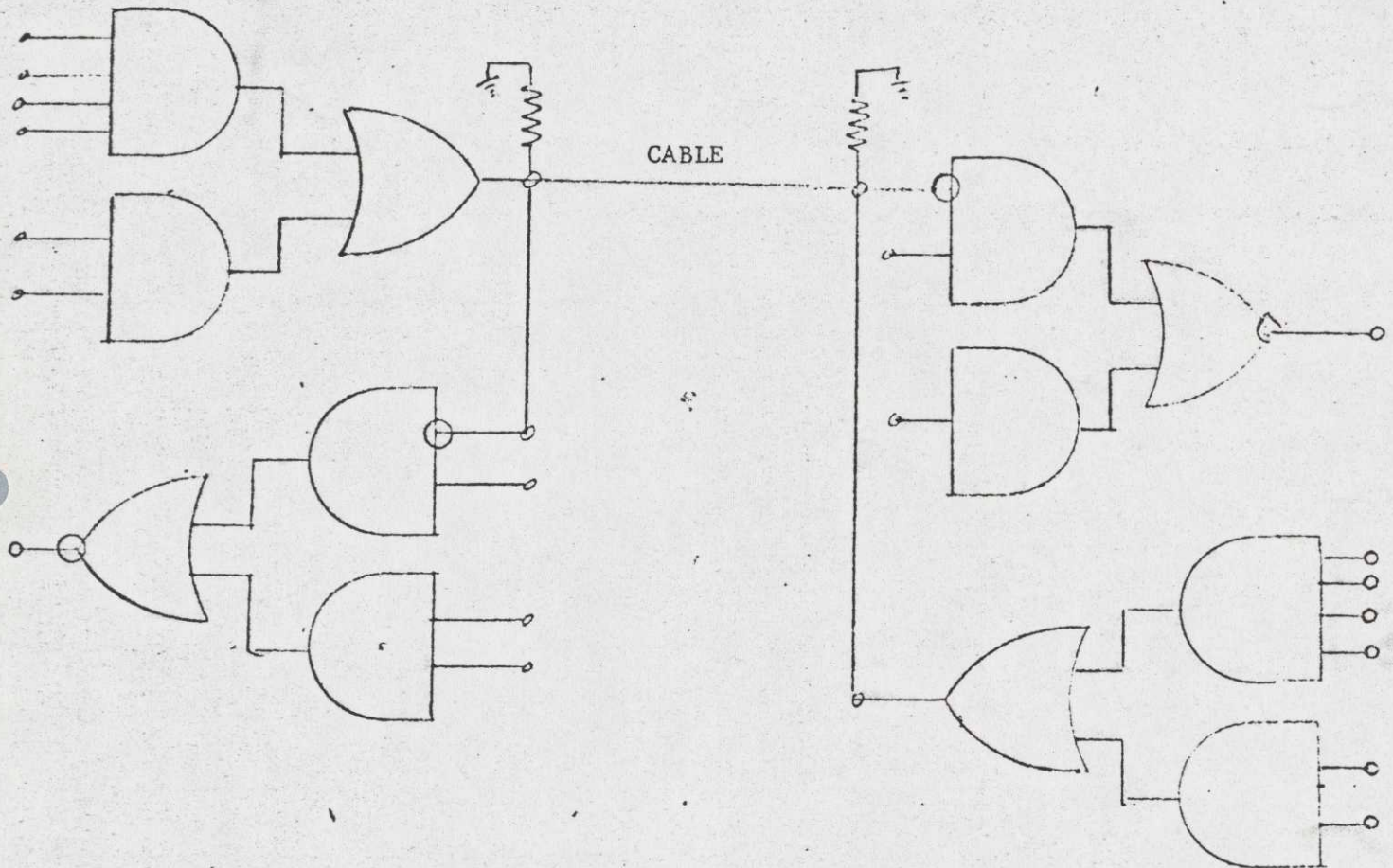


FIGURE 5.1-F PSI CIRCUITS, BI-DIRECTIONAL DATA

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6.0 T&D AND MAINTAINABILITY CONSIDERATIONS

There are no special features of this interface related specifically for Test and Diagnostic (T&D) and Maintainability. It is felt that the PST dialog, channel programs, etc., will look the same to the CPU I/O hardware/firmware for normal operation and for T&D; any special diagnostic meaning shall be between the MPC and CPU diagnostic software.

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